

Abstract of the Disclosure

A signal communication apparatus of a clock reproduction system in which clock signals are extracted from each of parallel data signals for redigitizing each of the data signals. The apparatus includes a reference clock signal generating circuit which is comprised of a clock extraction circuit for extracting a clock signal from each of a plurality of bits of received data signals, and a clock signal selection circuit for selecting one of the extracted clock signals. Alternatively, the reference clock signal generating circuit may be comprised of a data signal selection circuit for selecting one of a plurality of received data signals, and a clock extraction circuit for extracting a clock signal from the selected bit. Based on the resultant reference clock signal, clock signals are obtained that are phase-adjusted for redigitizing each bit of the received data signals. The selection made in the selection circuit is switched on the basis of the output of a clock signal monitoring circuit that detects the occurrence of abnormalities in the frequency of the extracted clock signal. Thus, the extraction of clock can be continued using other bits in the event of an abnormality in the bit from which the clock is being extracted.